

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 6,847,248 B2
APPLICATION NO. : 10/043763
DATED : January 25, 2005
INVENTOR(S) : Ajit

Page 1 of 13

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the Title Page

| | |
|-----------------------|---|
| (57) Abstract, line 1 | Delete "input output", Insert --input/output-- |
| (57) Abstract, line 3 | Delete "so does", Insert --so do-- |

In the Claims

| | |
|-----------------------------|--|
| Column 10, line 47, Claim 3 | Delete "not present", Insert --not present,-- |
| Column 11, line 11, Claim 4 | Delete "not present", Insert --not present,-- |
| Column 11, line 28, Claim 5 | Delete "not present", Insert --not present,-- |
| Column 11, line 57, Claim 6 | After "device", Insert --;-- |
| Column 12, line 19, Claim 7 | Delete "comprises" |
| Column 12, line 32, Claim 9 | After "Semiconductor) ", Insert --device-- |

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It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Drawings

| | |
|--------------------------|---|
| FIG. 4, Sheet 4 of 23 | Delete Drawing Sheet 4 and substitute therefore the Drawing Sheet, consisting of Fig. 4, as shown on the attached page |
| FIG. 6, Sheet 6 of 23 | Delete Drawing Sheet 6 and substitute therefore the Drawing Sheet, consisting of Fig. 6, as shown on the attached page |
| FIG. 9A, Sheet 9 of 23 | Delete Drawing Sheet 9 and substitute therefore the Drawing Sheet, consisting of Fig. 9A,, as shown on the attached page |
| FIG. 10, Sheet 11 of 23 | Delete Drawing Sheet 11 and substitute therefore the Drawing Sheet, consisting of Fig. 10, as shown on the attached page |
| FIG. 11A, Sheet 12 of 23 | Delete Drawing Sheet 12 and substitute therefore the Drawing Sheet, consisting of Fig. 11A, as shown on the attached page |
| FIG. 12A, Sheet 16 of 23 | Delete Drawing Sheet 16 and substitute therefore the Drawing Sheet, consisting of Fig. 12A, as shown on the attached page |

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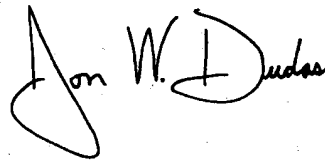
Page 3 of 13

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

| | |
|--------------------------|---|
| FIG. 12B, Sheet 17 of 23 | Delete Drawing Sheet 17 and substitute therefore the Drawing Sheet, consisting of Fig. 12B, as shown on the attached page |
| FIG. 13, Sheet 18 of 23 | Delete Drawing Sheet 18 and substitute therefore the Drawing Sheet, consisting of Fig. 13, as shown on the attached page |
| FIG. 14, Sheet 19 of 23 | Delete Drawing Sheet 19 and substitute therefore the Drawing Sheet, consisting of Fig. 14, as shown on the attached page |
| FIG. 18, Sheet 23 of 23 | Delete Drawing Sheet 23 and substitute therefore the Drawing Sheet, consisting of Fig. 18, as shown on the attached page |

Signed and Sealed this

Twenty-first Day of November, 2006

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looping initial "J" and a distinct "D".

JON W. DUDAS
Director of the United States Patent and Trademark Office

FIG. 4

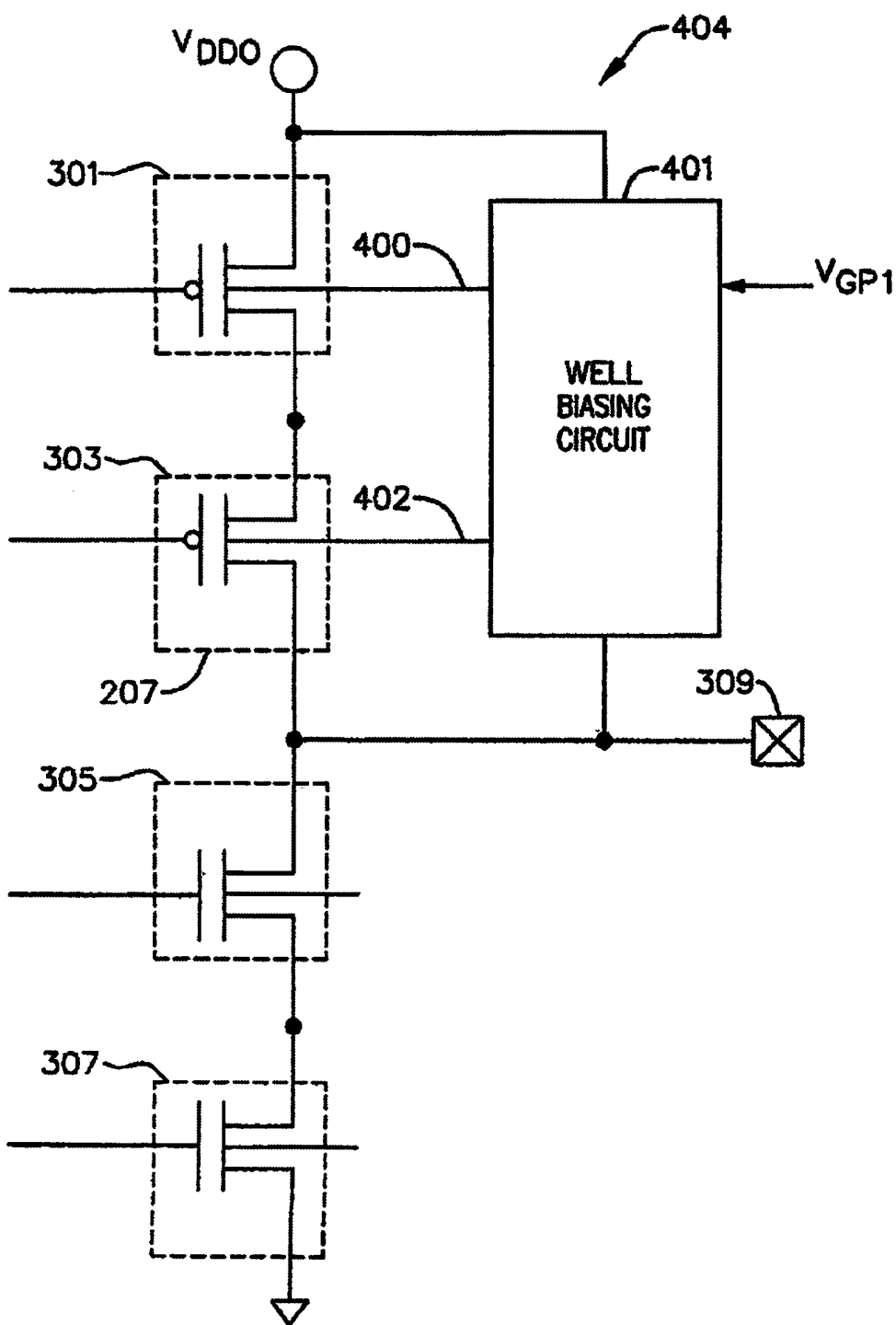


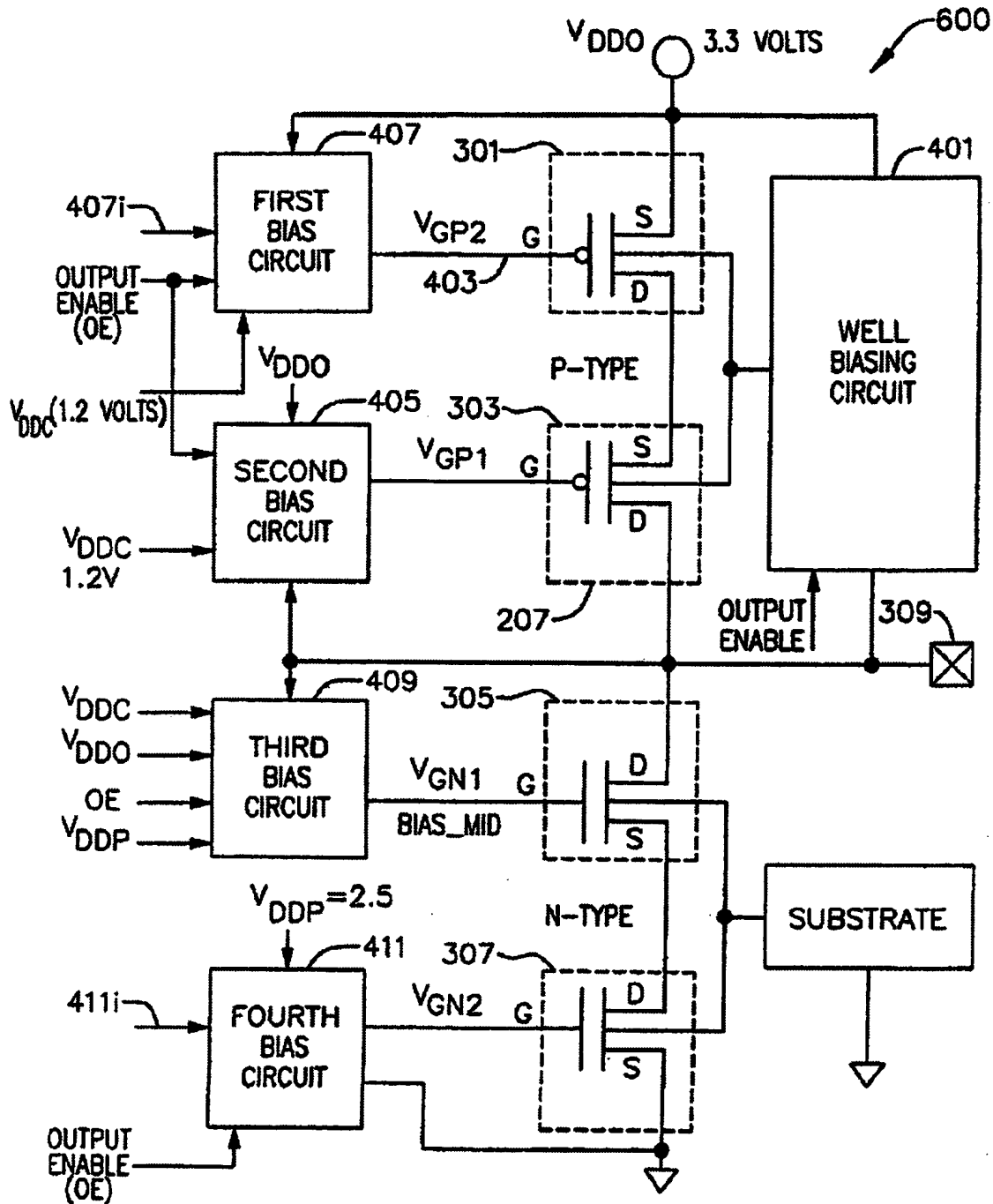
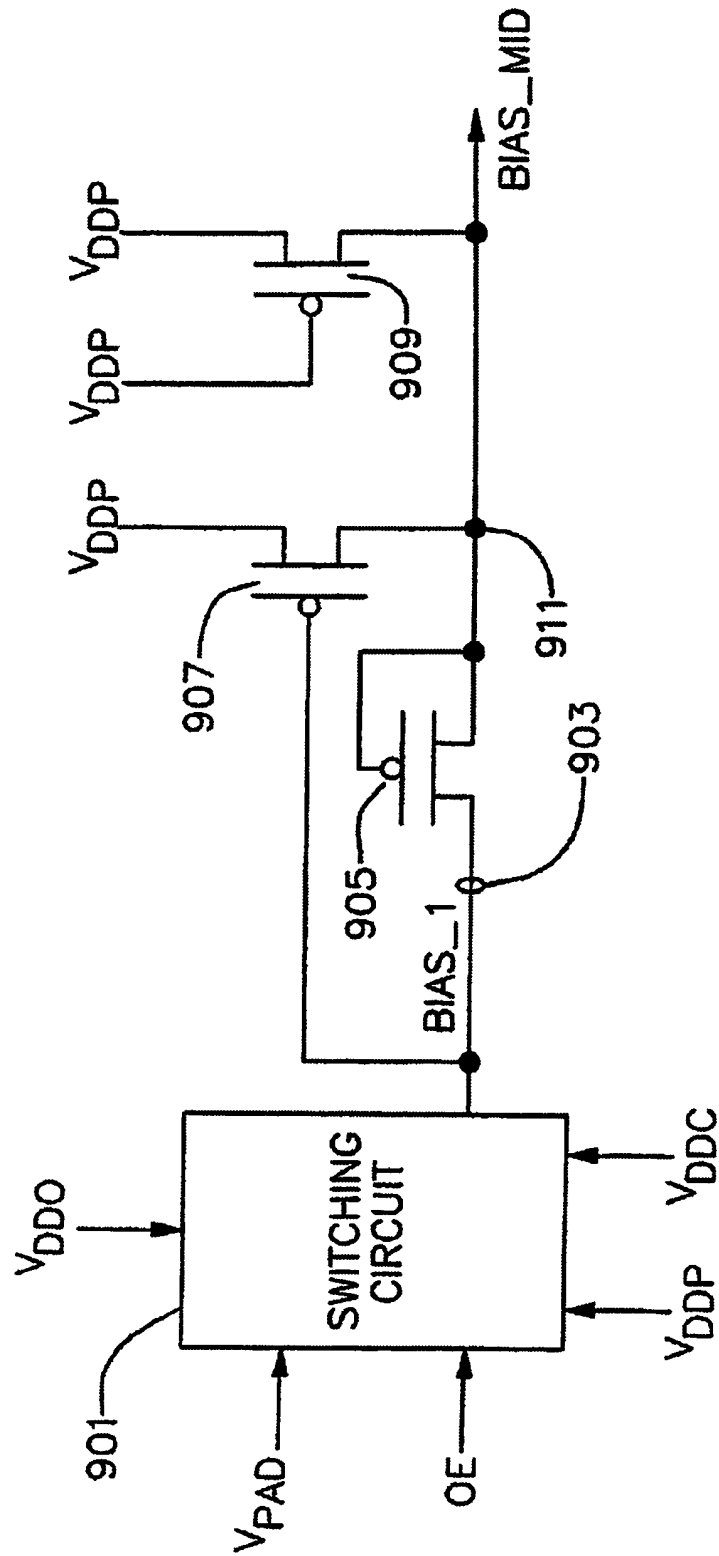
FIG. 6

FIG. 9A



The diagram shows a PMOS driver circuit. A PMOS transistor 1003 has its gate connected to a PMOS bias circuit 405, which is controlled by an output enable (OE) signal and a 1.2V V_{DDC} supply. The PMOS transistor 1003's source is connected to a V_{DDO} supply. Its drain is connected to a node 1005, which is also connected to a PMOS transistor 303. The gate of transistor 303 is connected to a first bias circuit 409, which is controlled by a 409 signal and a 407 supply. The source of transistor 303 is connected to a node 207. A well biasing circuit 401 is connected to the well of the PMOS transistor 1003 and the well of the PMOS transistor 303. The well biasing circuit 401 is controlled by a 401 signal and a 403 supply. The well biasing circuit 401 is also connected to a node 309, which is connected to a V_{PAD} supply. The node 309 is also connected to a node 1001, which is connected to a V_{DDO}-V_{TP} supply.

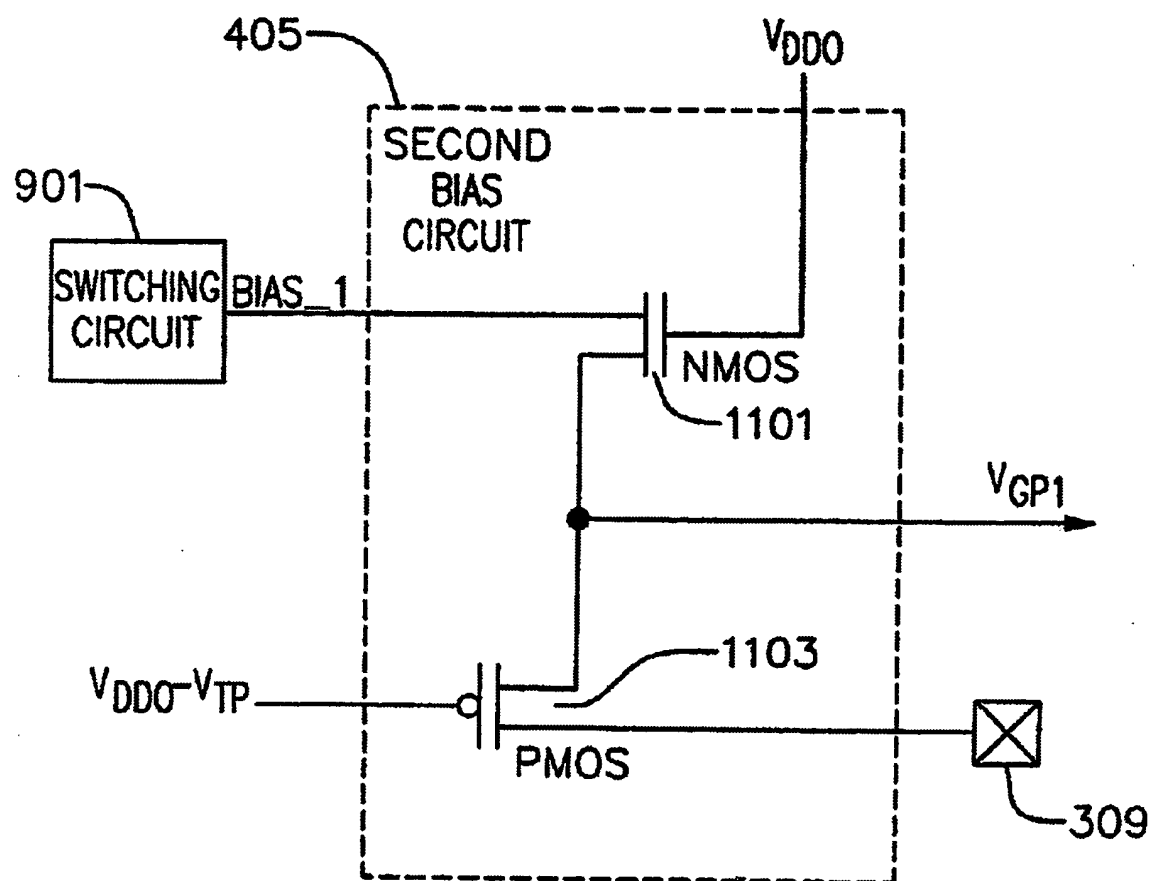
FIG. 11A

FIG. 12A

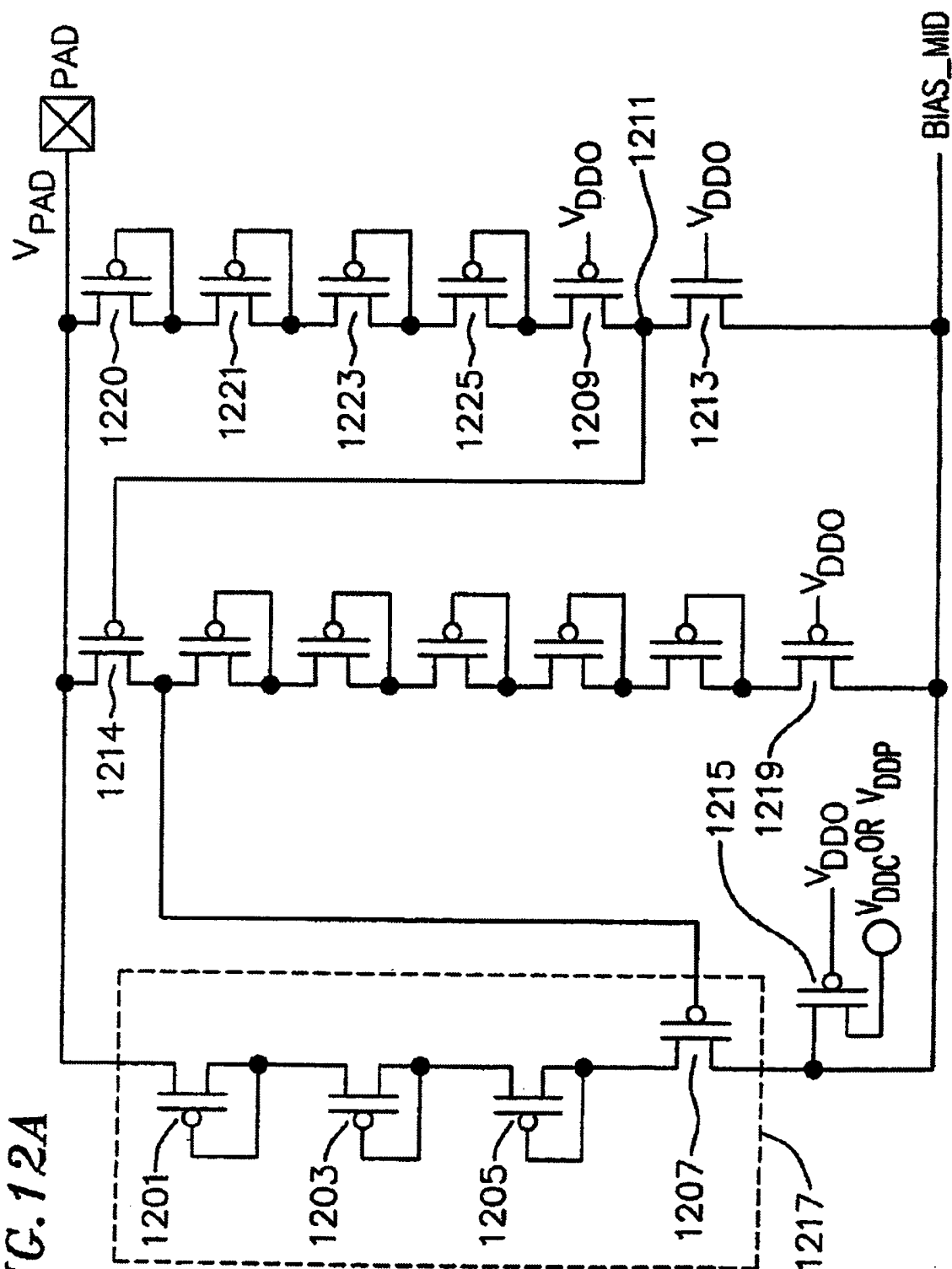


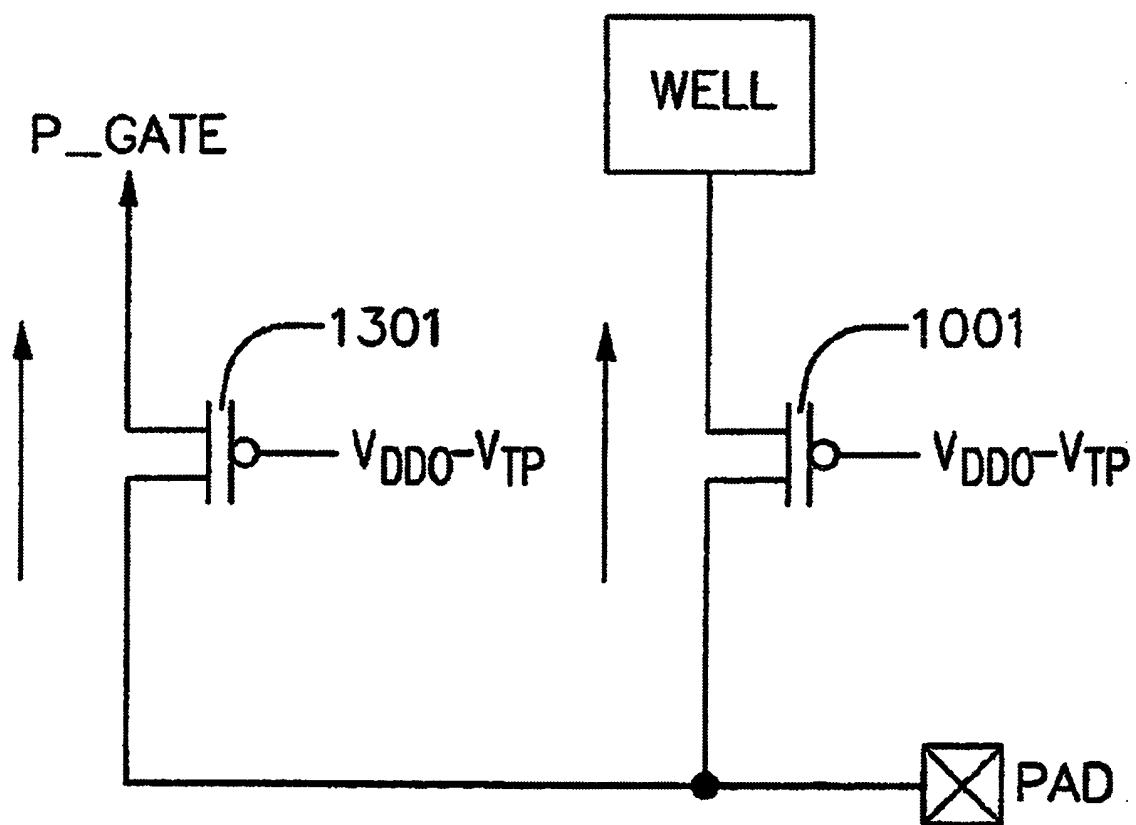
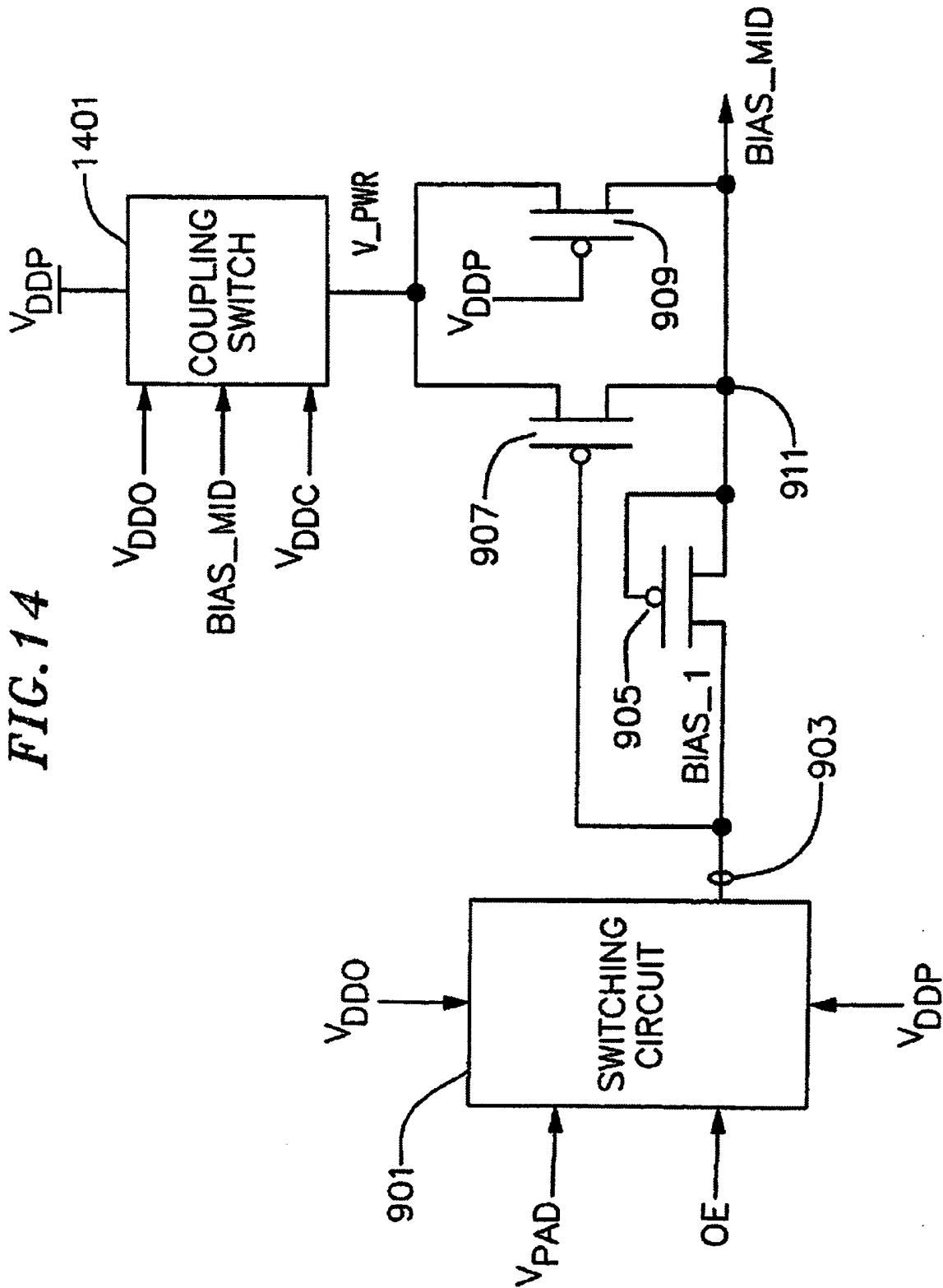
FIG. 13

FIG. 14



The circuit diagram illustrates a pixel driver circuit. At the top, a PMOS pre-driver (407) receives DATA and OE signals, with VDDO and VDDC supply rails. Its output is connected to a PMOS transistor (301) whose source is tied to VDDO and whose gate is connected to a node labeled VGP1. This node is also connected to a capacitor Cgp and a PMOS transistor (303) whose source is also VDDO. A node labeled 1800 is connected to the gate of 303 and to a load resistor (represented by a square with an X). Below this, a switching circuit (901) is controlled by OE and VDDC. It drives a node connected to a PMOS transistor (1201) and a network of other transistors (1203, 1209, 1220, 1213, 1214, 1219, 907, 1505, 1506, 1507). A BIAS_MID signal is applied to the gates of 1203, 1209, 1213, and 1219. A capacitor Cgd is connected between the output node and the gates of 1213 and 1219. A capacitor Cbm is connected between the output node and VDDO (305). The output node is also connected to a PMOS transistor (307) whose source is VDDO and whose gate is connected to a node labeled 307. At the bottom, an NMOS pre-driver (411) receives DATA and OE signals, with VDDP and VSSC supply rails. Its output is connected to an NMOS transistor (307) whose source is VSSC and whose gate is connected to the output node. A node labeled 909C is connected to the gates of 1201 and 1203, and to the gates of a stack of four NMOS transistors (910C, 911C, 912C) whose sources are connected to VSSC.